ABSTRACT OF THE INVENTION

An image processing architecture for a scanner, especially used to process the image data output from an analog signal processor by a digital controller, is provided. The image processing architecture of the present invention comprises a ping-pong buffer, an image data storage region and a cache memory. The ping-pong buffer has at least two buffer rows, any of which is used to store the image data. The image data storage region is used to store a correction parameter for image data correction and to store the image data corrected according to the correction parameters. The correction parameters obtained from the image data storage region are stored in the cache memory. The cache memory provides such correction parameters so that the above image data can be corrected in the image processing architecture according the image correction parameter. Additionally, the image processing architecture further includes a cache as a working buffer for line-difference compensation.